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Gate Coupling and Charge Distribution in Nanowire Field Effect Transistors

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ABSTRACT

We have modeled the field and space charge distributions in back-gate and top-gate nanowire field effect transistors by solving the three-dimensional Poisson's equation numerically. It is found that the geometry of the gate oxide, the semiconductivity of the nanowire, and the finite length of the device profoundly affect both the total amount and the spatial distribution of induced charges in the nanowire, in stark contrast to the commonly accepted picture where metallic dielectric properties and infinite length are assumed for the nanowire and the specific geometry of the gate oxide is neglected. We provide a comprehensive set of numerical correction factors to the analytical capacitance formulas, as well as to numerical calculations that neglect the semiconductivity and finite length of the nanowire, that are frequently used for quantifying carrier transport in nanowire field effect transistors.

In recent years, semiconductor nanowires (NWs) have come under extensive investigation for applications in high-performance electronic[1,2] and optical[3] devices. Nanowire field effect transistors (NWFETs) have demonstrated carrier mobilities close to or higher than in the bulk,[4−6] offering an intriguing alternative to thin film technology for high-speed electronics.[7]

In NWFETs, transistor ON−OFF behavior is achieved by applying a gate voltage that electrostatically induces free carriers in the NW channel. When the induced carriers are of the same type as the original doped carriers in the accumulation regime, there will be a measurable enhancement in electrical conductance. In the linear regime, the conductance is expressed as[8]

$$\frac{\partial I_{sd}}{\partial V_{sd}} = \mu \cdot \frac{C \cdot (V_{gate} - V_{threshold})}{L^2} \tag{1}$$

where μ is the majority carrier mobility, C the gate-NW capacitance, and L the gated NW length. For V_{gate} of reverse polarity, the doped carriers are repelled and the channel is depleted of majority carriers, reducing electrical conductivity; further change in the gate voltage results in the accumulation of free charge carriers with the opposite sign, i.e., inversion. The carrier mobility is determined from the NW conductance as a function of V_{gate}. It is therefore critical to know the gate-NW capacitance for accurate assessment of the carrier mobility and doping level.

Because of the extremely low capacitance and complications from local electrostatic effects, the gate-NW capacitance has only recently been measured through direct experimental means in a top-gate device geometry for carbon nanotubes[9] and in top-gate and surround-gate Ge NWFETs.[10] In typical back-gate NWFET geometries, an analytical formula derived from a metallic cylinder-plane system[11] is routinely used for calculating the gate-NW capacitance,[12−14]

$$\frac{C}{L} = \frac{2\pi\epsilon_0\epsilon_r}{\cosh^{-1}((R+h)/R)} \tag{2}$$

where h is the gate oxide thickness, R is the NW radius, and ϵ_r is the relative dielectric constant of the oxide. The denominator can be simplified to $\ln(2h/R)$ when $h \gg R$.[15] Three assumptions are made, however, in deriving eq 2: (1) The oxide fills the *entire* space surrounding the NW. This is much different from the widely used, conventional back-gate geometry, where the gate oxide exists only as a film separating the NW and the gate plane, leaving the NW fully exposed to air, which has $\epsilon_r = 1$. (2) The NW is *electrostatically metallic*, such that the entire NW and the electrodes are an equipotential and the induced charges exist only on the NW surface.[11] In reality, however, the NW is typically a semiconductor with nondegenerate doping and nonideal dielectric screening. (3) The NW is assumed to be *infinitely long*, such that the electric field distortion near the metal electrodes is neglected. However, because of the different

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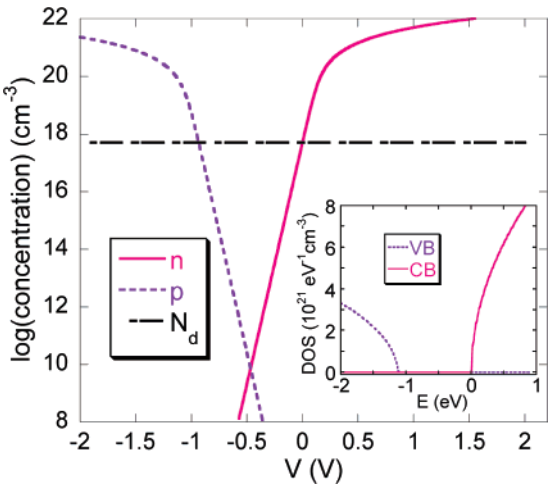

Figure 1. Electron and hole concentrations as a function of local potential in n-type Si doped with $N_d = 5 \times 10^{17}$ cm^{-3}. At $V = 0$, the Fermi level lies at its natural position with respect to the CB and VB edges such that n is equal to N_d to maintain charge neutrality. Inset: The density of states for conduction and valence bands of Si in the effective mass approximation. Here, for $N_d = 5 \times 10^{17}$ cm^{-3} and at room temperature, the natural Fermi level lies at $E_F = -0.11$ eV.

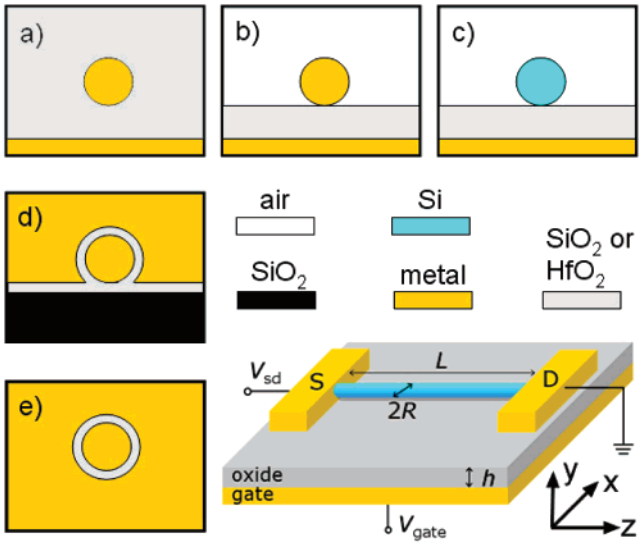

Figure 2. Cross-sectional schematic of different device models considered in this study. (a) Back-gate nanowire embedded (BE) model, (b) back-gate metallic (BM) model, (c) back-gate semiconducting (BS) model, (d) top-gate metallic (TM) model, and (e) surround-gate metallic (SM) model. A 3D schematic of the BS model is also shown with device dimensions. In the BE, BM, and BS models, h is the distance between the NW bottom surface and the gate plane; in the TM and SM models, h is the thickness of the oxide wrapping around the nanowire.

geometries and dielectric properties of the electrodes from those of the NW, an edge effect, known as the fringe capacitance, perturbs the gate-NW coupling when the NW has limited length.

These three assumptions limit the accuracy of the gate-NW capacitance evaluated from eq 2. The first limitation due to the oxide geometry has recently been numerically analyzed in *two dimensions* (2D), and a factor of 2 reduction in capacitance was found to account for this limitation.[16,17] Although the first assumption has recently been given increasing attention and corrected for in back-gate experiments,[5,16−20] the other two assumptions are typically ignored. A comprehensive set of calculations comparing all three limitations of eq 2 for both back-gate and top-gate NWFETs has yet to be reported. To gauge and compare the magnitude of all three limitations, we performed numerical simulations of a back-gate NWFET by solving the classical Poisson's equation in *three dimensions* (3D). Our model allows for a gate oxide in a film geometry, a semiconducting NW channel, and also a finite NW length. The capacitance, modeled as a function of device geometries and NW doping levels, is discussed in comparison to eq 2. Top-gate NWFETs are also simulated and compared to the back-gate devices.

As a representative example, we use n-type silicon as the NW material and SiO_2 (or HfO_2 later in the paper) as the gate oxide in the simulation. The surface of the NW is assumed to be fully passivated, such that surface Fermi level pinning and other surface effects can be neglected. The electron and hole concentrations are calculated as a function of local electric potential, as shown in Figure 1. This is achieved by integrating the density of states (DOS) in conjunction with the Fermi−Dirac distribution, where E_F is displaced by the potential, V, with respect to conduction band (CB) and valence band (VB) edges,

$$n(V) = \int_{-\infty}^{\infty} \frac{\rho_c(E)}{1 + \exp[(E - E_F - V)/k_B T]} dE \qquad (3)$$

Here $\rho_c(E)$ is the DOS of the 6-fold degenerate CB minimum of Si in the effective mass approximation,[21] and E_F is given by the charge neutrality condition at $V = 0$: $n(0) = N_d + p(0)$. A similar expression can be derived for $p(V)$, where the DOS includes the contribution from heavy-hole, light-hole as well as spin−orbit split-off VBs.[21] The DOS for both CB and VB are shown in the inset in Figure 1. Two distinct regimes are distinguishable: the nondegenerate regime where $\log(n)$ and $\log(p)$ exhibit a linear dependence on V in comparison with the nonlinear, degenerate regime where the bands are heavily populated. The crossing point of $\log(n)$ and $\log(p)$ when E_F is displaced to mid-bandgap defines an intrinsic free carrier concentration of $\sim 10^{10}$ cm^{-3} in Si at room temperature. In our simulations, we ignore quantum confinement effects and use the classical 3D density of states. We limit our simulations to Si nanowires with radius ≥ 10 nm. For these nanowires, our estimate shows that the spacings of the first few subbands are much smaller (<6 meV) than $k_B T$ at room temperature. Therefore, multiple subbands are populated as a consequence of thermal excitation, rendering quantum effects negligible and justifying our classical approximation.

The electric potential, $V(x,y,z)$, is given by the 3D Poisson's equation in our device geometry (Figure 2),

$$\vec{\nabla} \cdot [\epsilon \vec{\nabla} V(x,y,z)] = \rho(x,y,z) \qquad (4)$$

where the space charge density $\rho = q \cdot [N_d - n(V) + p(V)]$

in Si and is zero otherwise, and $\epsilon = \epsilon_0\epsilon_r$ with each dielectric material volume (Si, SiO_2, air) assigned with their respective values of ϵ_r. The metallic gate and source and drain electrodes are characterized with $\epsilon \rightarrow \infty$ to ensure that they are equipotential bodies with respect to the applied voltage. The contacts between the electrodes and the NW are assumed to be ohmic so that no potential drop associated with a Schottky barrier exists on the contacts.[22] We ignore work function differences between the electrode and gate metal and the semiconductor. For convenience of discussion, we define five different models (Figure 2): (I) The back-gate nanowire embedded (BE) model (Figure 2a) using the same assumptions as eq 2 to reproduce eq 2, with the oxide filling the *entire space* surrounding a *metallic* NW. The simulated capacitance from the BE model will be compared with the value calculated from eq 2 as a control for the simulation. (II) The back-gate metallic (BM) model (Figure 2b), where the gate oxide exists *only as a film* separating the NW and the gate plane, but the NW is still rendered electrostatically metallic. In this model, the first limitation to eq 2, which assumes the NW fully embedded in the gate oxide, is lifted. The simulated capacitance from this model will be compared with previously reported simulations. (III) The back-gate semiconducting (BS) model (Figure 2c) to represent the realistic back-gate NWFET, where the oxide exists only as a film separating the NW and the gate plane, and the NW is *semiconducting*, with space charge induction governed by eq 3. In this model both limitations to eq 2 are lifted. (IV) The top-gate metallic (TM) model (Figure 2d)[5,13] to compare with the back-gate devices. (V) The surround-gate metallic (SM) model (Figure 2e), which is commonly used in experiments to calculate the TM devices.

The simulation was carried out using the software FlexPDE, which is a finite element partial differential equation solver with a triangular mesh. The back gate is held at V_{gate}, and both the source and drain electrodes are grounded such that no current flows, ensuring a constant E_F in the NW. We model the device at $V_{sd} = 0$ to simulate the small-bias, linear regime where carrier mobility is usually determined in experiments. We solve for the potential with the Neumann boundary condition that the electric field perpendicular to the boundary planes $(\nabla\vec{V})_\perp$ is zero at the outer boundary of the entire simulation domain. We choose the domain to be sufficiently large such that the change in simulation results with further increase in domain size is negligibly small. The potential contours in the $z = 0$ plane for the BE, BM, and BS models simulated in 3D with identical parameters are shown in parts a, b, and c of Figure 3, respectively. As a consequence of both the different spatial arrangement of gate oxide (in both BM and BS models) and the semiconducting response in the NW (in the BS model), the potential distributions in these three models differ substantially. In the inset of each plot, a more detailed image of the NW potential distribution is shown. As expected, a nonuniform potential distribution is evident when the NW is semiconducting. In this case, the minimum potential occurs at a point off the center of the NW away from the gate. The potential reaches a maximum at the edge of the NW that touches the gate

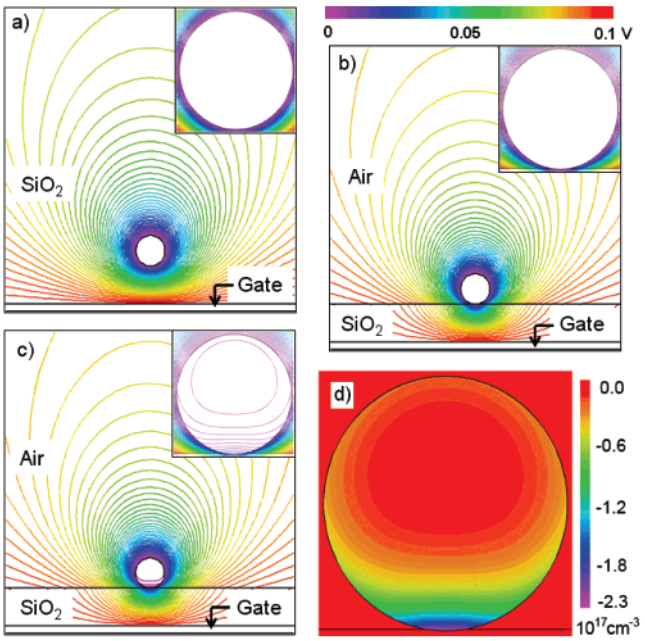

Figure 3. Equipotential contours of (x,y) cross-section plane at the center of the NW ($z = 0$) for the BE (a), BM (b), and BS (c) models. The displayed area is 400 nm × 400 nm, out of a simulation domain of 500 nm in both x and y directions. The color bar is shown above (b). A magnified image of the Si NW is shown in the inset (color scale different from main image), with equipotential contour lines 1 mV apart from each other. In (d), the net space charge distribution in the NW in the BS model is shown. These figures were generated by simulating with the following parameters: $R =$ 20 nm, $h = 50$ nm, $L = 1$ μm, $V_{gate} = 0.1$ V, and $N_d = 5 \times 10^{17}$ cm^{-3} (for the BS model).

oxide. The voltage drop in this NW cross section is about 10% of the total V_{gate}. The variation of V in the Si NW translates to a net space charge distribution $N_d - n(V) + p(V) \approx N_d - n(V)$ as shown in Figure 3d. As expected, dense negative space charges accumulate at the bottom of the NW due to the electrostatic attraction from the positive V_{gate}. However, the NW is largely charge neutral, with $n(V) = N_d$ as a result of charge screening. At smaller V_{gate} or lower N_d, this space charge distribution becomes more uniform because the NW channel becomes increasingly nonmetallic. This space charge picture differs considerably from the metallic-NW model implied by eq 2, where induced charge would exist only on the NW surface, and also from the picture of uniform charge distribution commonly assumed in analysis of carrier transport in the NW cross section. Therefore, the effect of semiconducting properties must be considered in the discussion of device performance in the NWFETs, such as charge transport, quantum confinement, photoexcitation, and recombination.

Now we turn to the effect of finite NW length. Because of the edge effect, the electric field is severely distorted near the electrodes. The potential distribution along the side-view (y,z) plane is shown in Figure 4 for two devices, one with a NW of length 500 nm (main) and the other with a NW of length 50 nm (inset). A stronger variation of V along z around the NW is evident for the shorter device. This comparison highlights the necessity of performing 3D simulations for devices with finite length. Moreover, for the semiconducting

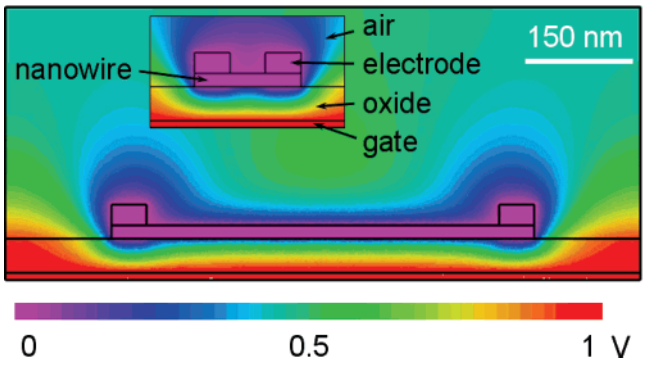

Figure 4. Electric potential distribution in the (y,z) plane in the BM model to show the potential variation along the NW due to the edge effect. In the simulation, the following parameters were used: $R = 10$ nm, $h = 50$ nm, $L = 500$ nm (main) or 50 nm (inset), $V_{gate} = 1.0$ V, oxide is SiO_2, and the electrodes have dimensions of 500 nm (length), 50 nm (height) and 50 nm (width) in x, y, and z directions, respectively.

model, 3D simulation is required *even for a long NW device*: A sufficiently long NW in the metallic models can be approximately simulated in 2D in the (x,y) plane where, as a boundary condition, the entire NW is at the same potential as the electrodes (grounded). In the semiconducting model, however, such a boundary condition does not exist to justify a simplified 2D simulation, and inputs from 3D simulation are required to locate the minimum potential point in the (x,y) plane, as shown in the inset of Figure 3c.

To compare these models in a quantitative manner, we determine the gate-NW capacitance by calculating the electrostatic energy stored in the system,

$$\frac{1}{2}C \cdot V_{gate}^2 = \int \frac{1}{2}\epsilon_0\epsilon_r[\nabla \vec{V}(x,y,z)]^2 \, dx \, dy \, dz \qquad (5)$$

To model the capacitance with minimum disturbance from the edge effect, we construct the device in 3D (Figure 2) and choose a sufficiently long NW ($L = 1$ μm) to solve eq 4 (this choice of length will be justified later in the paper). A thin (x,y) plane slice in the middle of the NW (at $z = 0$), where the field distribution is nearly a constant along z-direction, is sampled. The integration in eq 5 is limited to this slice, and the capacitance per unit length is obtained from dividing C by the thickness of the slice. For the metallic models where the NW is an equipotential body with the electrodes, eq 5 precisely defines the capacitance between the gate and the NW. However, for the semiconducting model where the potential varies inside the NW, the capacitance between the NW and the gate is no longer well defined. As such, for practical purposes, we define the capacitance of the middle slice using the total space charge induced within the slice divided by the voltage difference between the gate (V_{gate}) and the electrodes (grounded),

$$C = \frac{q}{V_{gate}} \cdot \int [N_d - n(V) + p(V)] \, dx \, dy \, dz \qquad (6)$$

This definition allows one to determine the amount of induced charge in the NW at given V_{gate} using eq 1 for practical conductance calculation.

In Figure 5a, we show the simulated capacitance for all three back-gate (BE, BM, and BS) models as a function of V_{gate}. As expected, BE and BM capacitances remain constant when V_{gate} varies. The control, the simulated BE capacitance, agrees within 2% with the analytical expression eq 2. The deviation is caused by the limited size of the simulation domain. Consistent with previous reports based on 2D simulations,[16,17] BM capacitance is significantly lower than BE (for these system parameters, by ~48%), indicating a large overestimation of the capacitance for back-gate NWFETs when using eq 2. This results in both an underestimation of the carrier mobility and an overestimation of the doping level approximately by a factor of 2. Figure 5a also shows BS capacitance calculated from eq 6. It approaches BM value in the accumulation regime ($V_{gate} > \sim 1$ V), as expected from the nearly metallic electrostatics in the NW. However, as the NW moves into the depletion regime with increasingly negative V_{gate}, BS deviates severely from BM, decreasing to <65% of BM (<32% of BE) near the threshold voltage, reflecting weaker charge screening in the depleted NW. Such a capacitance decrease from ON to OFF state is well-known in planar metal-oxide-semiconductor field-effect transistors[8] and has recently been experimentally observed in top-gate Ge NWFETs.[10] At further negative V_{gate}, the n-type NW enters the inversion regime, where the valence bands start to be populated by free holes and the capacitance increases back toward BM.

We calculated these three capacitances (BE, BM, and BS) in the small V_{gate} limit as a function of N_d and NW radius R, while keeping h constant. The dependencies are shown in Figure 5b, where the capacitance is normalized to the calculated value from eq 2 and R is normalized to h. It can be seen that, in the range of R/h investigated (0.1−0.8), BM capacitance differs significantly from BE and hence a correction factor must be considered when using eq 2 to calculate the gate-NW capacitance in back-gate NWFETs. This factor defines an "effective" ϵ_r for the entire system, encapsulating the contributions of both the SiO_2 and air. This "effective" ϵ_r can be used to lift the gate oxide geometry limitation of eq 2, restoring the validity of eq 2 for the BM model. Many groups have implemented this correction to eq 2 in calculating experimental mobility,[18,20] citing an average dielectric constant between the oxide and air. It should be noted, however, that although a simple mathematical average between dielectric constants of SiO_2 and air happens to approximately correct for NWs with all diameters, such a simple mathematical average does *not* result in the appropriate correction for high-ϵ_r oxides as shown below. Additionally, when the semiconductivity (and finite length) of the NW are accounted for, one sees in Figure 5 (and Figure 6) that using a constant "effective" ϵ_r does not properly adjust for the capacitance at all values of V_{gate}, N_d, R, and NW length.

The N_d dependence in Figure 5b quantifies the second limitation of eq 2 that neglects the semiconductivity of the NW. As demonstrated in Figure 5a,b, this correction is

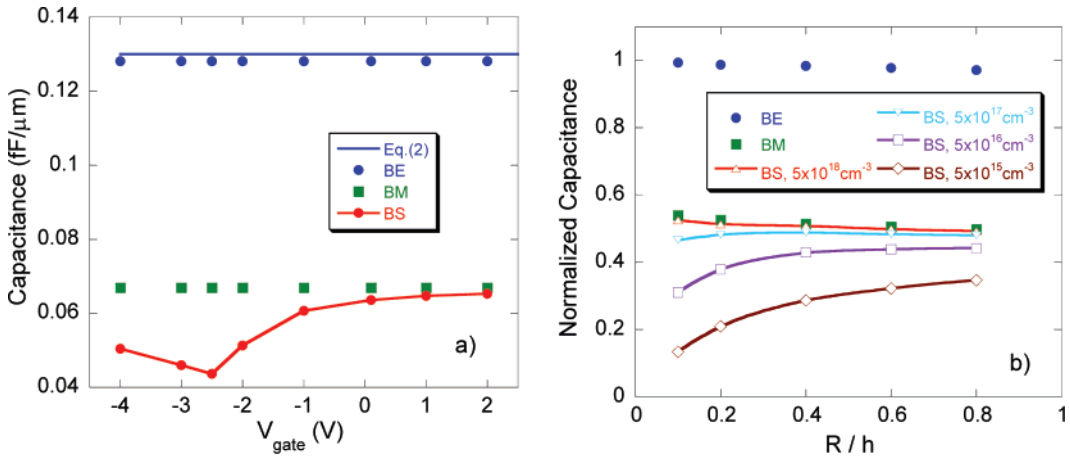

Figure 5. (a) Capacitance per μm of NW length obtained as a function of V_{gate} from the simulation of the BE, BM, and BS models. Also shown is the capacitance calculated from eq 2 for the BE model. The parameters used were $R = 20$ nm, $h = 50$ nm, $L = 1$ μm, and a gate oxide of SiO_2. For the BS model, $N_d = 5 \times 10^{17}$ cm^{-3}. (b) Capacitance normalized to the analytical value calculated from eq 2 as a function of R normalized to h over a wide range of N_d. The parameters used were $h = 50$ nm, $L = 1$ μm, and $V_{gate} = 0.1$ V. We note that for the points at $R/h = 0.1$, quantum confinement effects are expected to modify the capacitance values from these shown data with classical calculations.

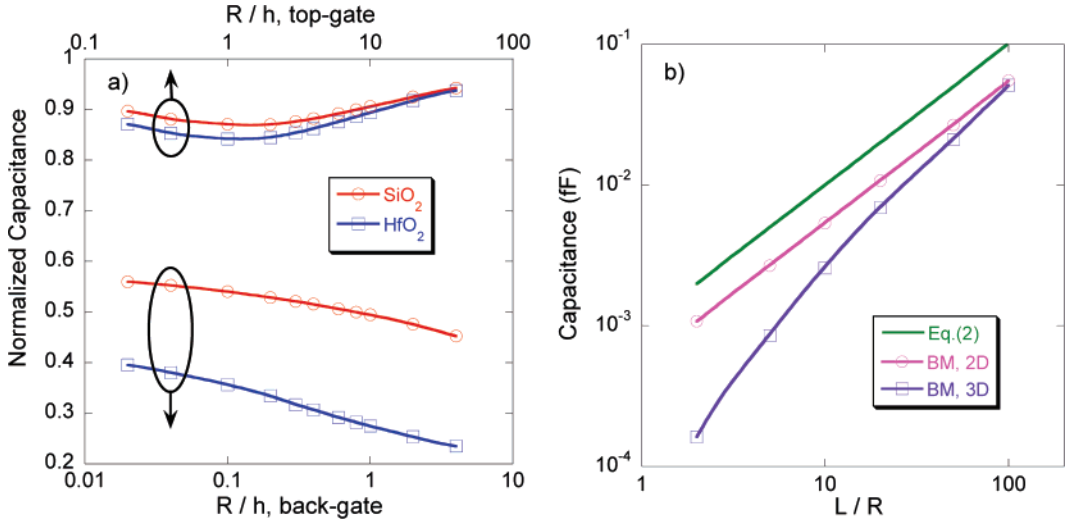

Figure 6. (a) Normalized gate-NW capacitance as a function of R/h for the BM (bottom axis) and TM (top axis) models using SiO_2 and HfO_2 as the gate oxide. Note the different scale for these two axes. Here the BM and TM capacitances are normalized to the value calculated from eqs 2 and 7, respectively. In the simulation, $h = 50$ nm, $L = 1$ μm, and $V_{gate} = 0.1$ V. (b) Capacitance between the back gate and the gated NW as a function of L/R for the BM model. In the simulation, $h = 50$ nm, $R = 10$ nm, and $V_{gate} = 0.1$ V, and gate oxide is SiO_2.

negligibly small for $N_d > \sim 5 \times 10^{17}$ cm^{-3} in the strong accumulation regime ($V_{gate} > \sim 1$ V). However, this factor becomes significant and must be included when $N_d < \sim 5 \times 10^{17}$ cm^{-3}, or when the device is operated near the threshold V_{gate}. This effect is stronger for NWs with smaller radii, consistent with results from Vashaee et al.,[17] where 2D simulations of nonideal conducting cylinders of different diameters were performed. Parts a and b of Figure 5 show the fundamental limitations to accuracy one can achieve in simulating the capacitance when the NW is modeled as a perfect conductor. Because this difference is caused by the semiconducting properties of the NW, rather than the device geometry, it is expected to be present in top-gate and surround-gate devices as well.

In advanced NWFET technologies using high-ϵ_r materials as the gate oxide, these correction factors are found to be even more drastic and cannot be corrected by the simple mathematical averaging as can be done for SiO_2 and air. For example, by using the device parameters in Figure 5a but replacing SiO_2 ($\epsilon_r \sim 4.5$) with HfO_2 ($\epsilon_r \sim 22$), BM capacitance is further reduced from 52% to 31% of BE. This ratio is shown as a function of R/h in Figure 6a. Also shown in Figure 6a is the capacitance of the TM device,[5,13] normalized by the value expected from a perfect surround-gate metallic (SM) device,

$$\frac{C}{L} = \frac{2\pi\epsilon_0\epsilon_r}{\ln((R+h)/R)} \tag{7}$$

It can be seen that the correction to the top-gate device is much smaller than that to the back-gate devices due to the closer resemblance between the TM and SM geometries.

The finite length effect is calculated by comparing the BM model in both 2D and 3D, as shown in Figure 6b. Here we

used the BM instead of the BS model in order to decouple the semiconductivity and short-channel effects and highlight separately these factors that both affect gate capacitance. As per Figure 5b, a metallic channel can be safely assumed in simulation of the realistic, semiconducting channel when $N_d > \sim 10^{18}$ cm^{-3}. In the 2D simulation, the entire NW is grounded for solving the Poisson's equation in 2D, and the capacitance is calculated from eq 5. This capacitance is found to be identical to the value obtained in the 3D "slice method" for long NWs described above. This capacitance applies to the back-gate device with an infinitely long NW. For the 3D situation, Gauss' law was applied to the entire NW channel (but not electrodes) to compute the total charge (Q) induced within the NW, and the gate-NW capacitance was obtained from $C = Q/V_{gate.}$ As expected, the 3D capacitance deviates considerably from a linear scaling with L for short L. At $L = 1$ μm (i.e., aspect ratio of NW is $L/R = 100$), the 3D capacitance agrees well with the 2D capacitance, indicating a negligible edge effect. At $L = 20$ nm ($L/R = 2$), the 3D capacitance is only 16% of the 2D value. Here the fringe capacitance effect is quantitatively exemplified using one size of the source−drain electrodes while varying the channel length. Previous work[23] on carbon nanotube transistors has demonstrated how the size and shape of source−drain contacts affect the capacitance. We expect similar capacitance variation with respect to electrode size and shape in NWFETs. Figure 6b therefore quantifies the third limitation of eq 2 due to the electrostatic screening of electrodes when the NW channel is short.

In summary, by solving the Poisson's equation in 3D, we have calculated the gate coupling and charge distribution in nanowire field effect transistors. Our simulation yields sizable corrections to the analytical formulas and calculations by neglecting semiconducting properties and finite length of the NW commonly used to evaluate gate−nanowire capacitance in both back-gate and top-gate devices and calls for similarly large corrections in analyzing carrier mobility and concentration in nanowire field effect transistors.

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